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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/811,666	03/20/2001	Ki-Whan Song	SEC.807	9403

7590 10/23/2002

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EXAMINER	
PAREKH, NITIN	
ART UNIT	**PAPER NUMBER**
2811	

DATE MAILED: 10/23/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

A-6

Office Action Summary	Application N .	Applicant(s)	
	09/811,666	SONG, KI-WHAN	
	Examiner	Art Unit	
	Nitin Parekh	2811	

-- The MAILING DATE of this communication appears on the cover sh et with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 August 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) *5-10* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4 and 11-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *4* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

1. Claims 1-4 and 11-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over the admitted prior art (APA) in view of Masakuni et al (Japanese Pat. 10-284678), Stearns et al (US Pat. 5895967) and Kirkman (US Pat. 6064113).

Regarding claim 1, the APA discloses a ball grid array (BGA) package/chip scale package (CSP) semiconductor device with two or more external powers including a first and second power, the device comprising:

- a semiconductor chip having a plurality of conventional pads including power, ground, etc. arranged along a center of a surface
- a substrate having a slot of a predetermined size and centrally arranged in a spaced relationship to the pads, the substrate having a signal line plane including signal line patterns having a plurality of power, ground and signal balls mounted

on the respective ball mounts to be connected to an external circuit on its one side and the chip being mounted on the other side, and

- a bonding material being inserted between the chip and the substrate to fix the chip to the substrate

(Fig. 1A, 1B and 2; specification pages 1-3).

The APA fails to specify the signal line plane being divided into two or more planes including a first plane having only a first power lines and a second plane having only a second power lines.

Masakuni et al teach using a substrate having a variety of power/signal/ground routing configurations comprising a signal plane (5c in Fig. 2, 14-18, 1-18) where the signal plane is divided into two planes including a first and second plane (5c-1 and 5c-2 in Fig. 2, 14-18, etc.) located on a first and second portions of the substrate surface where each portion is on opposing sides of the slot (5C-1 and 5C-2 in Drawing 2, 14, etc.) to provide a design flexibility and optimization for power and ground electrodes and respective routing. Masakuni et al further teach each planes having any desired level/combination of power/ground potentials so that the first plane/combined plane has only a first combined power lines and a second plane/combined plane has only a second combined power or ground lines (English translation- sec. 0018, 0040, 0041, 0066-0070; Fig. 1-17).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the signal line plane being divided into two or more planes including a first plane having only a first power lines and a second plane having only a second power or ground lines so that the number and routing of power and ground electrodes can be optimized for improved electrical performance and reliability using Masakuni et al's signal plane routing in the APA.

Regarding claims 2-4, the claim elements have been addressed in the rejection as explained above for claim 1.

Regarding claim 11, the claim elements have been addressed in the rejection as explained above for claim 1.

Regarding claims 12 and 13, the APA fails to specify a boundary defining the power or ground plane wrapping around signal ball mounts positioned on the respective planes and interconnection lines.

Masakuni et al teach dividing the power and ground planes into sections/piles/boundaries (Drawings 14-17; sec. 0070).

It is conventional in the chip scale packaging and interconnection technology art to select parameters such as number/spacing of ball/mount/pad connections, number of power/ground/signal layers, a layout/pattern of such connections in each layer, etc. to achieve the desired noise/cross-talk reduction, grounding and signal distribution for the

device. Stearns et al and Kirkman teach using conventional routing layout/design where the power and ground planes wrap around power, ground or signal ball mounts and interconnection lines at any desired level in the substrate (Stearns et al - Fig. 3; Col. 5 and 6; Kirkman- Fig. 4 and 5; Col. 7 and 8) to achieve the optimized routing and electrical performance.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the boundary defining the power or ground plane wrapping around signal ball mounts positioned on the respective planes and interconnection lines so that the routing for the power and ground electrodes can be optimized to improve the electrical performance using Stearns et al and Kirkman's routing design in the APA.

Regarding claims 14 and 15, the APA discloses a conventional layout where the power or ground balls/mounts are formed on both sides of the slot in a mixed pattern and are being separated from the respective planes (Fig. 1A/B and 2; specification pages 1-3).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nitin Parekh whose telephone number is 703-305-3410. The examiner can normally be reached on 09:00AM-05:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on 703-308-2772. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7722, 703-308-7724 or 703-872-9318 (Right FAX) for regular communications; 703-872-9310 (Right FAX) for After Final communications and 703-872-9310 (Right FAX) for customer service.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-306-3431.

Nitin Parekh

NP
10-18-02

Tom Thomas

TOM THOMAS
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